SELF-REPAIRING REDUNDANCY FOR MEMORY BLOCKS IN PROGRAMMABLE LOGIC DEVICES

ABSTRACT

Programmable logic devices (PLDs) including self-repairing RAM circuits, and methods of automatically replacing defective columns in RAM arrays. A RAM circuit including redundant columns is tested during the PLD configuration sequence using a built in self test (BIST) procedure. If a defective column is detected, an error flag is stored in an associated volatile memory circuit. After the BIST procedure is complete, the PLD configuration process continues. The presence of the error flag causes the configuration data to bypass the defective column and to be passed directly into a replacement column. The configuration process continues until the remainder of the circuit is configured, including the redundant column. In other embodiments, the BIST procedure is initiated independently from the PLD configuration process. When a defective column is detected, user operation resumes with data being shunted from the defective column to a redundant column in a fashion transparent to the user.